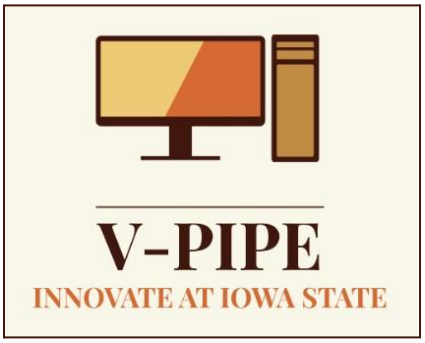

EE/CprE/SE 4920 BI-WEEKLY REPORT 3

09/20/2024 – 10/03/2024
Group number: 6
Project title: Video Pipeline for Machine Vision
Client: JR Spidell
Advisor: Dr. Phillip Jones

Team Members: Ritwesh Kumar (Video Stream to FPGA), Deniz Tazegul (Video Stream to FPGA), Liam Janda (VDMA to DDRM), Taylor Johnson (DDRM to Displayport)

o Bi-Weekly Summary

The team has created a configuration code for the IMX219 image sensor, MIPI D-PHY and CSI-2 blocks, and VDMA components in a Jupyter Notebook file. The team continues to monitor the MIPI D-PHY and CSI-2, as well as VDMA status bits, to determine if the IMX219 video data is being sent to DDR memory and output to a DisplayPort monitor as desired.

o Past two week accomplishments

- **Deniz:** Worked with the other group members to ensure correct MIPI configuration and set up sequence. Updated MIPI testing to be more comprehensive, including continuous testing for frequently changed bits and registers. Looked more into the STOP STATE signal and the implications of receiving that at the physical layer.
- **Liam:** Worked with Ritwesh to change the MIPI code to follow the programming sequence detailed in the CSI-2 and D-PHY datasheet. Looked into why the frames were not able to be viewed in DDRM.
- **Taylor:** Met with Deniz and Ritwesh to better understand updates to the MIPI and camera configuration code. Worked with Ritwesh to determine whether frames are being stored in DDR memory. Updated the code using the MMIO class. Ran a test that plots the frame to observe the output for the TPG VDMA code. The output matches what is expected. Then, this test was added to the full pipeline code and tested. The output was zeros. Taylor also reviewed the IMX219 status registers to determine which registers would be useful in debugging the code.

- **Ritwesh:** Helped update the code in a Jupyter Notebook file to reflect the programming sequence recommended by the MIPI D-PHY and CSI-2 block and VDMA component datasheets. He observed that the long packets in the MIPI CSI-2 block continually increase to 0xFFFF before resetting to 0, meaning multiple video lines are sent from the IMX219. He looked into the PYNQ VDMA read frame function. Along with Taylor, he helped to successfully read data manually, using the PYNQ MMIO library, from DDR memory, which may be useful for debugging the IMX219 video stream data. He also added IMX219 status registers to the team's pipeline slides. He checked the Ultra96-v2 daughter board datasheet and helped verify that the port used for the IMX219 is compatible with the MIPI protocol.

o **Pending issues**

There are no pending issues at this time.

o **Individual contributions**

Name	Individual Contributions	Hours this Report	Cumulative Hours
Deniz	MIPI programming sequence, MIPI debugging, MIPI testing	10	25
Liam	MIPI programming sequence, DDRM debugging	10	30
Taylor	Tested the TPG VDMA and full pipeline codes to read from DDR memory, and reviewed status registers for the IMX219 image sensor.	6	25
Ritwesh	Added IMX219 status registers to the team's pipeline slides, helped create code following the programming sequence suggested by the MIPI D-PHY and CSI-2 blocks and VDMA component datasheets, and observed the MIPI CSI-2 long packet count increase to 0xFFFF and reset to 0 meaning multiple	15	37

	video lines are received from the IMX219 to the MIPI CSI-2 block.		

o **Plans for the upcoming two weeks**

- **Deniz:** Keep working to get coherent video to DDR memory, test the new overlay
- **Liam:** Continue to work with the team to get the IMX219 data through to the DDR memory. Test the new overlay.
- **Taylor:** Work with the team to test the new overlay. Will reach out to ETG to set up Vivado on senior design lab computers. Work on using the ILA to debug the MIPI block.
- **Ritwesh:** Work with the team to test different overlay configurations and monitor status register bits for the MIPI D-PHY and CSI-2 blocks, and the VDMA component. Work on reading data from DDR memory from the IMX219.

Action Item	Task Owner	Expected Date
Monitor the MIPI D-PHY and CSI-2 blocks, and VDMA status register bits when using different overlay configurations	All	10/17
Check if any data is received in DDR memory from the IMX219	All	10/17

o **Summary of bi-weekly advisor meeting**

The team had its first scheduled recurring bi-weekly advisor meeting. During the meeting, the team received feedback on ways of debugging the pipeline including monitoring MIPI D-PHY and CSI-2 blocks and VDMA status registers, looking into using an integrated logic analyzer (ILA), and ensuring that the connection between the IMX219 and Ultra96-v2 FPGA is correct for transmitting sensor data through the MIPI protocol. The advisor also recommended looking into how the PYNQ read frame function works to read data from DDR memory for debugging purposes.